UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/083,502	02/27/2002	Takayuki Tamura	XA-9639	6495

181 7590 11/01/2005

MILES & STOCKBRIDGE PC
1751 PINNACLE DRIVE
SUITE 500
MCLEAN, VA 22102-3833

EXAMINER	
TABONE JR, JOHN J	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 11/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/083,502	TAMURA ET AL.	
	Examiner	Art Unit	
	John J. Tabone, Jr.	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 8-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 8-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 January 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-5 and 8-13 remain in the current application and have been examined. Claims 1, 2, 8, 9, and 13 have been amended.

Response to Amendment

2. In the amendment filed 08/04/2005, the Applicants failed to provide page and line numbers in the specification where the new limitations of amended claims 1, 2, 8, 9, and 13 are supported. After performing a detailed search of the specification the Examiner cannot find where the new claim limitations are supported. As such, the new claim limitations are being considered as new matter and unsupported by the specification, subject to a 35 U.S.C. § 112, first paragraph rejection as failing to comply with the written description requirement. Further, these new claim limitations will not be considered and further examined on the merits. The Applicants are reminded, however, that upon provision of the supporting documentation and correction of the 35 U.S.C. § 112, second paragraph rejections the Examiner will reconsider the claim limitations and examine them on the merits.

As a result, the Examiner maintains the current rejection of claims 1-5 and 8-13 as set forth in the Final Office Action of Record dated 05/04/2005.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-5 and 8-13 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

After performing a detailed search of the specification the Examiner cannot find where the new claim limitations of amended claims 1, 2, 8, 9, and 13 are supported. As such, the new claim limitations are being considered as new matter and unsupported by the specification. The Applicants are required to provided page and line numbers in the specification where the new limitations of amended claims 1, 2, 8, 9, and 13 are supported.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-5 and 8-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1, 2, 8, 9 and 13:

These claims recite the limitation "said first address of a second non-volatile memory". There is insufficient antecedent basis for this limitation in the claim.

Claims 1 and 8:

These claims recite the limitation "when said second address of said second non-volatile memory is invalid". There is insufficient antecedent basis for this limitation in the claim. The Examiner cannot speculate whether this limitation would be "when said second address of said first non-volatile memory is invalid" or "when said third address of said second non-volatile memory is invalid". As is these claims will not be further examined on the merits.

Claim 2:

These claims recite the limitation "and said second address of said second non-volatile memory do not include an error memory cell". There is insufficient antecedent basis for this limitation in the claim.

Claims 3-5 and 10-12:

These claims are also rejected because they depend on claims 1, 8 and 9 and have the same problems of insufficient antecedent basis.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-5 and 8-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Estakhri et al. (US-6202138), hereinafter Estakhri.

Claims 1 and 2:

Estakhri teaches Memory card 502 includes: a non-volatile memory bank 506 including a plurality of non-volatile memory units 508 for storing sectors of information organized in blocks; a memory controller 510 coupled to the memory bank via a memory bus 512, and coupled to the host 504 via a host bus 514. Estakhri also teaches controller 510 is shown to include: a host interface 610 connected to the host 504 via host bus 514 for transmitting address, data, and control signals (external access instruction) between the controller and the host. Estakhri further teaches memory bus 512 is used to transmit address, data, and control signals between the controller 510 and memory bank 506. (Col. 6, lines 9-14, 28-61). Estakhri even further teaches that sector-organized information (alternation control), including user data and overhead information, is received at host interface 610 from host 504 via host bus 514 and provided to the data buffer 614 for temporary storage. (Col. 7, lines 28-30). Estakhri

discloses that the even and odd sector move flag locations 760, 762 store values indicating whether the corresponding even and odd sectors stored in the non-volatile memory sector location have been moved to another location within the non-volatile memory bank 506 (FIG. 6). (Col. 9, lines 53-67). Estakhri discloses "said memory controller allocates said first and second non-volatile memories to storage area of even and odd data of sector data", per claim 2, in column 8, lines 26-55. Estakhri also discloses the controller 510 (FIG. 6) accesses an even sector of information stored collectively in the first and second flash memory chips by simultaneously accessing first and second even sector fields 734, 742 (operate for parallel access) of corresponding row-portions of the first and second flash memory chips via the first and second split buses 680, 684 (FIG. 6), respectively. (Col. 8, lines 66, 67, col. 9, lines 1-5). Estakhri also discloses controller 510 (FIG. 6) monitors the status of each block location 727 of the memory bank using block level flags including a used/free block flag and a defect block flag stored in a used flag location 754 and a defect flag location 756 respectively of the flag field 752. Estakhri further discloses the following steps in Fig. 12a to teach "said memory controller makes the storage area alternative in unit of the non-volatile memory in which an access error occurs in said alternative control": At step 1600, the block that was being unsuccessfully programmed is marked as "defective" by setting the "defect" flags 756 (in FIG. 7). At step 1602, the space manager within the controller is commanded to find a free block. At step 1604, the information that would have been programmed at steps 1234 and 1222 (in FIG. 12) i.e. the block marked "defective" is programmed into corresponding sector locations within the free block found in step

1602. At step 1606, the block marked "defective" is checked for the presence of any sector information that was previously written thereto successfully. If any such sectors exist, at step 1608, these previously-programmed sectors are moved to the free block, as is additional block information in the process of FIG. 12. (Col. 9, lines 18-32, col. 17, lines 64-67, col. 18, lines 1-10). Estakhri discloses "a plurality non-volatile memories having management information used for performing alternation control " and "alternation control being performed individually for each of said plurality of non-volatile memories" in Fig. 11 which illustrates the alternative memory storage format, as depicted in FIG. 7, for storing a block of information in memory bank 506 (FIG. 6) wherein a single sector is written to a particular memory row location of the memory bank. Estakhri also discloses field 764 is a three bit field which is used for storing the old row flag in the first bit place, the used/free row flag in the second bit place, and the defect row flag in the third bit place. Estakhri further discloses field 766 is a two bit field which is used for storing the even sector move flag in the first bit place and the odd sector move flag in the second bit place (management information used for performing alternation control). (Col. 13, l. 59 to col. 14, l. 2).

Claim 3:

Estakhri teaches Memory bus 512 includes a flash bus 675 connected to a port 676 of memory I/O unit 652 for transmitting address, data, and command signals between flash memory chips 670, 672 and the memory I/O unit 652. (Col. 6, lines 59-64).

Claims 4 and 5:

Estakhri teaches an error correction code logic unit (ECC logic unit) 660 having a port 662 coupled to a port 664 of the flash state machine, and a port 666 coupled to a port 668 of the data buffer 614. Estakhri also teaches ECC logic block 660 includes circuitry for performing error coding and correction on the sector-organized information (adding an error detection code to write data) and performs error detection and/or correction operations on the user data portions of each sector stored in the flash memory chips 670, 672 or data received from host 504 (error detection and correction for read-data). Estakhri further teaches, by way of illustration in Fig. 9, the timing of control, address, and data signals for a write operation performed by memory system 600 (FIG. 6) wherein two sectors of information are simultaneously written in the non-volatile memory bank 506 (FIG. 6) during a single write operation. Estakhri discloses that immediately after time t10, during an interval between time t10 and a time t11, the first flash signal (wave form 902) transmits four packets of filler information (FFH, hexadecimal F, equivalent binary value "1111," decimal value "15") to the first flash memory chip via the first split bus 680 (FIG. 6) while the second flash signal (wave form 904) transmits error correction codes (ECC) to the second flash memory chip via the second split bus 684 (FIG. 6) (said ECC circuit conducts an input/output operation at an operation frequency equal to an input/output operation frequency of said parallel access operated non-volatile memories). (Col. 6, lines 46-49, col. 7, lines 41-46, col. 11, lines 7-12, col. 12, lines 36-43).

Claim 8 and 9:

Estakhri teaches Memory card 502 includes: a non-volatile memory bank 506 including a plurality of non-volatile memory units 508 for storing sectors of information organized in blocks; a memory controller 510 coupled to the memory bank via a memory bus 512, and coupled to the host 504 via a host bus 514. Estakhri also teaches controller 510 (control circuit) is shown to include: a host interface 610 connected to the host 504 via host bus 514 for transmitting address, data, and control signals (external access instruction) between the controller and the host; a memory input/output unit 652 (memory controller) having a port 654 coupled to a port 656 of the flash state machine. Estakhri further teaches memory bus 512 is used to transmit address, data, and control signals between the controller 510 and memory bank 506. (Col. 6, lines 9-14, 28-61). Estakhri even further teaches that sector-organized information (alternation control), including user data and overhead information, is received at host interface 610 from host 504 via host bus 514 and provided to the data buffer 614 for temporary storage. (Col. 7, lines 28-30). Estakhri discloses that the even and odd sector move flag locations 760, 762 store values indicating whether the corresponding even and odd sectors stored in the non-volatile memory sector location have been moved to another location within the non-volatile memory bank 506 (FIG. 6). (Col. 9, lines 53-67). Estakhri discloses "said memory controller allocates said first and second non-volatile memories to storage areas of even and odd data of sector data", per claim 9, in column 8, lines 26-55. Estakhri also discloses the controller 510 (FIG. 6) accesses an even sector of information stored collectively in the first and second flash memory chips by

simultaneously accessing first and second even sector fields 734, 742 (operate for parallel access) of corresponding row-portions of the first and second flash memory chips via the first and second split buses 680, 684 (FIG. 6), respectively. (Col. 8, lines 66, 67, col. 9, lines 1-5). Estakhri also discloses controller 510 (FIG. 6) monitors the status of each block location 727 of the memory bank using block level flags including a used/free block flag and a defect block flag stored in a used flag location 754 and a defect flag location 756 respectively of the flag field 752. (Col. 9, lines 18-32, col. 17, lines 64-67, col. 18, lines 1-10). Estakhri teaches "a control circuit that fetches a plurality of (first and second as per claim 9) management information from a plurality of non-volatile memories" in that controller 510 (FIG. 6) monitors the status of each memory row location 728 of the memory bank using flags including a used/free row flag stored in the used flag location 754, a defect row flag stored in the defect flag location 756 (error-related non-volatile memory), an old row flag stored in an old flag location 758 of the flag field 752, an even sector move flag stored in an even sector move flag location 760, and an odd sector move flag stored in an odd sector move flag location 762 (control circuit that fetches a plurality of management information). (Col. 9, ll. 33-52). Estakhri also teaches the control circuit "performs an alternation control for substituting a storage area of an access error-related non-volatile memory with another storage area", as recited in independent claims 8 and 9 is shown in FIG. 12a where the steps are performed by the microprocessor if the defect management routine at steps 1237 and 1225 (in FIG. 12) is executed. The block management routine is executed when the write operation is not successfully verified; the block(s) being programmed is in some

way defective and a different area in the nonvolatile memory, i.e. another block need be located for programming therein. At step 1600, the block that was being unsuccessfully programmed is marked as "defective" by setting the "defect" flags 756 (in FIG. 7) (error-related non-volatile memory). At step 1602, the space manager within the controller is commanded to find a free block (alternation control for substituting a storage area). At step 1604, the information that would have been programmed at steps 1234 and 1222 (in FIG. 12) i.e. the block marked "defective" is programmed into corresponding sector locations within the free block found in step 1602. At step 1606, the block marked "defective" is checked for the presence of any sector information that was previously written thereto successfully. If any such sectors exist, at step 1608, these previously-programmed sectors are moved to the free block, as is additional block information in the process of FIG. 12. (Col. 17, l. 56 to col. 18, l. 10).

Claims 10 and 11:

Estakhri teaches an error correction code logic unit (ECC logic unit) 660 having a port 662 coupled to a port 664 of the flash state machine, and a port 666 coupled to a port 668 of the data buffer 614. Estakhri also teaches ECC logic block 660 includes circuitry for performing error coding and correction on the sector-organized information (adding an error detection code to write data) and performs error detection and/or correction operations on the user data portions of each sector stored in the flash memory chips 670, 672 or data received from host 504 (error detection and correction for read-data). Estakhri further teaches, by way of illustration in Fig. 9, the timing of control, address, and data signals for a write operation performed by memory system

600 (FIG. 6) wherein two sectors of information are simultaneously written in the non-volatile memory bank 506 (FIG. 6) during a single write operation. Estakhri discloses that immediately after time t10, during an interval between time t10 and a time t11, the first flash signal (wave form 902) transmits four packets of filler information (FFH, hexadecimal F, equivalent binary value "1111," decimal value "15") to the first flash memory chip via the first split bus 680 (FIG. 6) while the second flash signal (wave form 904) transmits error correction codes (ECC) to the second flash memory chip via the second split bus 684 (FIG. 6) (said ECC circuit conducts an input/output operation at an operation frequency equal to an input/output operation frequency of said parallel access operated non-volatile memories). (Col. 6, lines 46-49, col. 7, lines 41-46, col. 11, lines 7-12, col. 12, lines 36-43).

Claim 12:

Estakhri teaches memory system 10 including a controller 12, which is generally a semiconductor (or integrated circuit) device, coupled to a host 14 which may be a PC or a digital camera. (Col. 1, lines 46-49).

Claim 13:

Estakhri teaches Memory card 502 includes: a non-volatile memory bank 506 including a plurality of non-volatile memory units 508 for storing sectors of information organized in blocks; a memory controller 510 (control circuit) coupled to the memory bank via a memory bus 512 (a bus), and coupled to the host 504 (external device) via a host bus 514. Estakhri also teaches controller 510 is shown to include: a host interface 610 (external interface) connected to the host 504 via host bus 514 for transmitting

address, data, and control between the controller and the host. Estakhri further teaches memory bus 512 includes a flash bus 675 connected to a port 676 of memory I/O unit 652 for transmitting address, data, and command signals between flash memory chips 670, 672 and the memory I/O unit 652 (plurality of I/O terminals). Estakhri even further teaches flash bus 675 includes 16 bit lines, 8 bit lines of which form a first bus 680 connected to a port 682 of I/O register 671 of the first flash memory chip, and another 8 bit lines of which form a second bus 684 connected to a port 686 of I/O register 673 of the second flash memory chip (bus has a first bus width...). (Col. 6, lines 9-14, 28-67). The claim limitation "said control circuit performs access control..., and performs address alternating processing..." is rejected per claim 1 and 2 above. Estakhri discloses "a plurality non-volatile memories having management information used for performing alternation control " and "address substitution being performed individually for each of said plurality of non-volatile memories" in Fig. 11 which illustrates the alternative memory storage format, as depicted in FIG. 7, for storing a block of information in memory bank 506 (FIG. 6) wherein a single sector is written to a particular memory row location of the memory bank. Estakhri also discloses field 764 is a three bit field which is used for storing the old row flag in the first bit place, the used/free row flag in the second bit place, and the defect row flag in the third bit place. Estakhri further discloses field 766 is a two bit field which is used for storing the even sector move flag in the first bit place and the odd sector move flag in the second bit place (management information used for address substitution). (Col. 13, l. 59 to col. 14, l. 2).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (571) 272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John J. Tabone, Jr.
Examiner
Art Unit 2133

10/13/05

GUY LAMARRE
PRIMARY EXAMINER